31. The method of claim 26 wherein said hint information directs said data to (a) a first way destination when said data is expected to be loaded but not reused extensively or said data is expected to be stored or modified but not reused extensively, and (b) a second way destination when data is expected to be loaded and reused extensively or said data is expected to be stored or modified and reused extensively.

REMARKS

Claims 20-31 are pending in the present application for the Examiner's consideration. Applicants have amended Claims 20 and 26. In accordance with the Examiner's request, the Applicants have updated the status information and application numbers for the co-pending applications referenced in the specification of the present application. No new matter has been added.

In summary of the Office Action of July 16, 2002, the Examiner has:

I. Rejected Claims 20-21 and 26-27 under 35 U.S.C. §103(a) as being unpatentable over *Baum et al.*, U.S. Patent No. 4,928,239, ("*Baum*") in view of *DeLano et al.*, U.S. Patent No. 5,396,604, ("*DeLano*"); and

II. Rejected Claims 22-25 and 28-31 under 35 U.S.C. §103(a) as being unpatentable over *Baum* in view of *DeLano*, and further in view of *Chi*, U.S. Patent No. 5,784,711, ("*Chi*").

Applicants respectfully traverse the Examiner's rejections.

I. Rejection of Claims 20-21 and 26-27 under 35 U.S.C. §103(a)

The Examiner rejected claims 20-21 and 26-27 as unpatentable under *Baum* in view of *DeLano*. The Applicants respectfully submit that Claims 20-21 and 26-27 are patentable over *Baum* in view of *DeLano* because the references fail to disclose or suggest all of the elements of the pending claims. For example, Claim 20 recites, in part:

forming an address to access data in a cache, wherein said address is formed by using information contained in said offset and base fields; and

prefetching said data, when unavailable in said cache, in accordance with hint information contained in said hint field, wherein said hint information indicates an expected use of said data and a destination for said data. (Emphasis added).

Claim 26 recites a similar limitation. Both of these claims call for prefetching data specified by an address contained in the instruction. The instruction further contains hint information indicating a destination for the data specified by the instruction. It is respectfully submitted that none of the cited references disclose or suggest using hint information in an instruction to indicate the destination of the data that is also specified by the instruction.

Baum discloses a system having a multiple-set cache memory structure. (*Baum*, Col. 2, lines 61-62; Figure 2). According to *Baum*, each "instruction executed by processor 19 . . . includes a number of bits which comprise a cache control specifier." (*Baum*, Col. 5, lines 23-26). The cache control specifier "specifies the method to be used in swapping data from the cache." (*Baum*, Col. 5, lines 34-35). The cache "responds to these specifiers to choose the replacement scheme best suited for the type of data specifies." (*Baum*, Col. 5, lines 34-35).

Baum discloses that when the "NORMAL" cache control specifier is invoked, "the cache operates according to the standard replacement scheme, in this case, LRU [Least Recently Used]." (*Baum*, Col. 5, lines 43-45). The "STACK" cache control specifier does the opposite, marking recently accessed (and thus no longer needed) stack entries as "least recently used." This deallocates the cached stack space by making unneeded stack entries more eligible for replacement. (*Baum*, Col. 6, lines 5-10). The "SEQUENTIAL" specifier operates the cache in a similar fashion. (*Baum*, Col. 6, lines 28-30).

Baum uses these three cache control specifiers to indicate whether the data in the cache referenced by an instruction should be replaced. Since the data referenced by the instruction is already in the cache (otherwise it could not be marked for

replacement), these cache control specifiers do not indicate a destination for the data referenced by the instruction. It is true that a future instruction may prefer to store data in a cache location indicated by a cache control specifier of the present instruction. However, the cache control specifiers of *Baum* do not indicate a destination for data referenced by the present instruction.

Baum also discloses a "PREFETCH" cache control specifier. Unlike the other cache control specifiers, this cache control specifier indicates that, "in a LOAD or STORE to a first block, the next block, that is the block immediately following the first block in main memory, is very likely to be accessed in the near future." (*Baum*, Col. 6, lines 34-38). In response, the cache "performs a normal LOAD or STORE and fetches the next block if it is not already in the cache. (*Baum*, Col. 6, lines 38-40). The "PREFETCH" specifier does not mark any cache data for replacement.

Baum uses the "PREFETCH" cache control specifier to specify a source of data (the next block from main memory), not the destination. As mentioned above, *Baum* discloses a multiple-set cache memory. Data from a given memory address can be stored in any one of the cache sets. Since the "PREFETCH" specifier does not mark any cache data for replacement, this specifier does nothing to indicate any preference for a particular destination. Thus, when the next block from main memory is retrieved in response to a "PREFETCH" specifier, the cache can store this information in any of the cache sets.

Similarly, *DeLano* does not disclose or suggest the cited elements of Claims 20 and 26. *DeLano* discloses a computer system having a data cache memory that "decodes an instruction requiring the CPU to load a value into a read only general purpose memory register, the instruction thereby indicating to the CPU to perform a prefetch operation." (*DeLano*, Abstract). *DeLano* does not disclose or suggest the use of a hint field in an instruction, let alone "prefetching said data . . . in accordance with hint information contained in said hint field" as required by Claims 20 and 26.

Since neither *Baum* nor *DeLano* disclose or suggest "forming an address to access data in a cache . . . and prefetching said data . . . in accordance with hint

information contained in said hint field, wherein said hint information indicates an expected use of said data and a destination for said data," as required by Claims 20 and 26, it is respectfully submitted that Claim 20 and 26 are patentable over *Baum* in view of *DeLano*. Furthermore, Claims 21 and 27 are patentable by virtue of their dependence on patentable independent claims.

II. Rejection of Claims 22-25 and 28-31 under 35 U.S.C. §103(a)

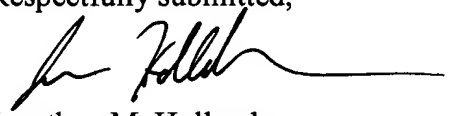
The Examiner rejected claims 22-25 and 28-31 as unpatentable under *Baum* in view of *DeLano*, and further in view of *Chi*. The Applicants respectfully submit that Claims 22-21 and 26-27 are patentable over the cited references due to their dependence on patentable independent claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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APPENDIX

IN THE SPECIFICATION:

A preferred embodiment of the present invention is incorporated by reference in a superscaler processor identified as "R10000," which was developed by Silicon Graphics, Inc., of Mountain View, California. Various aspects of the R10000 are described in commonly-owned copending patent applications having serial numbers: 08/324,124 ("Cache Memory"), 08/324,127 ("Redundant Mapping Tables"), 08/324,128 ("Memory Translation"), 08/324,129 ("Address Queue") and 08/404,625 **[(attorney docket number 012178-563-1]**, filed March 14, 1995, entitled "Address Queue"**[)]**, which are hereby incorporated by reference in their entirety for all purposes.

IN THE CLAIMS:

20. (Presently Amended) A method comprising:

issuing an instruction, wherein said instruction includes a hint field, a base field and an offset field;

forming an address to access data in a cache, wherein said address is formed by using information contained in said offset and base fields; and

prefetching said data, when unavailable in said cache, in accordance with hint information contained in said hint field, wherein said hint information indicates an expected use of said data and a destination for said data.

26. (Presently Amended) A method comprising:

issuing an instruction, wherein said instruction includes a hint field, a base field and an index field;

forming an address to access data in a cache, wherein said address is formed by using information contained in said index and base fields; and

prefetching said data, when unavailable in said cache, in accordance with hint information contained in said hint field, wherein said hint information indicates an expected use of said data and a destination for said data.